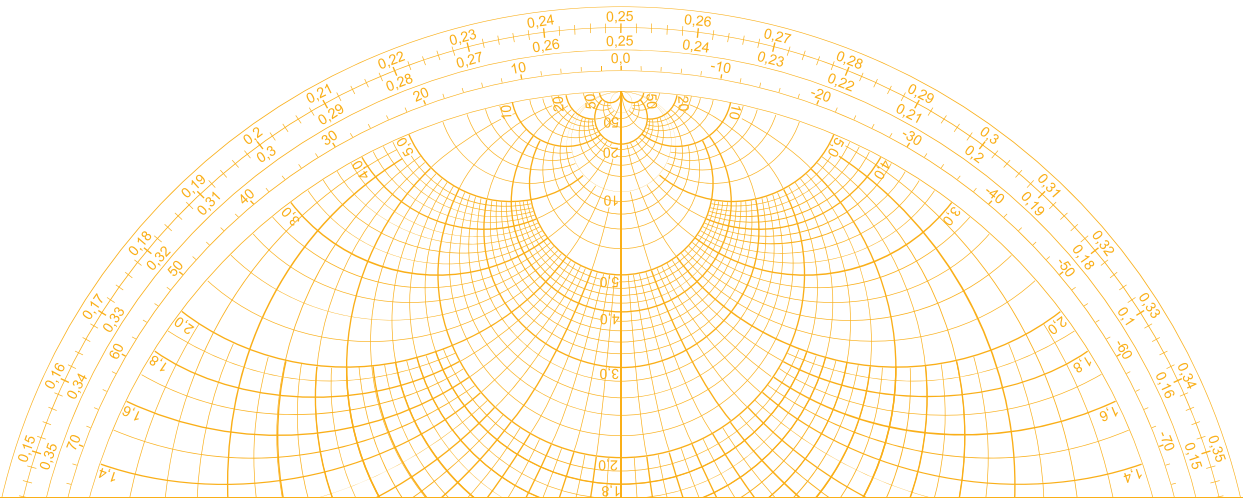




Signal and Power Integrity Course

4-day (36 study hours) course



RF Training



Test Equipment



RF Components & Systems



Engineering Services



RF Ventures Incubator

RF is our Business... Signal us!

Signal and Power Integrity Course

Introduction

High speed digital signals are essentially broadband RF signals by nature, which need to propagate through a PCB or a system with a minimal distortion. The signal quality or Signal Integrity ("SI") can easily deteriorate due to multiple mechanisms, such as attenuation, crosstalk, mode conversion, poor impedance matching, jitter, dispersion and other causes. As a result, the overall Bit Error Rate (BER) is increased, while EMC test failures and product reliability problems emerge. These problems lead to extended development time, repetitive layouts, numerous reproductions and a waste of budget.

Moreover, Signal Integrity in high speed digital ICs is highly effected by the Power Supply's quality. This calls for strict Power Delivery Network (PDN) design and analysis from the die (silicon) to the Voltage Regulator Module on the PCB which is known as Power Integrity (PI).

This training course deals with Signal and Power integrity of high speed digital signals.

The topics include:

- Design and analysis of SI from PCB to system level and PI in the PCB level.
- Practical Design Guidelines for PCB design in multi restricted environment.
- Extensive SIPI theory and practice, demonstration of the studied material with the help of dozens of examples from simulations and measurements.
- Briefing on data sheets and common specifications
- Familiarizing with SIPI simulation and measurement tools.
- SI proof of design and failure investigations.
- Qualification in defining Layout instructions for proper SIPI.

Presenter

The lecturer: Mr. Dror Haviv - has a M.Sc degree in electrical engineering focused in electromagnetism and microwaves. He is one of the leading SIPI engineers in Israel and known to have years of teaching experience in the SIPI field. Dror serves as an expert SIPI engineer and a researcher. As part of his job, Dror qualifies, trains and supervises many engineers in the SIPI field on a daily basis. Beyond his extensive SIPI knowledge he also has a deep familiarity with various types of simulation tools and test equipment.

Target audience

All professional engineers that are involved in design, qualification and manufacturing of products that contain high speed digital signals, such as: board design, layout, SIPI, verification, system and process manufacturer engineers.

Course Duration

4 days (36 hours) from 8:30-17:30

Course Structure

The course includes extensive theoretical and practical background, examples from simulations and measurements, review of datasheets and specifications, open discussions etc.

Course Syllabus * Subject to changes *

1. Introduction

- Introduction to Signal Integrity
- The Band Width (BW) of deterministic digital signals (Knee Frequency)
- The important harmonics in deterministic signals, Spread Spectrum Clock (SSC)
- Power Spectral Density (PSD) of random digital data signals
- The Nyquist Frequency
- The BW of random digital signals (PRBS and Coded)
- Properties of Electromagnetic TEM waves in PCBs
- Lumped vs Distributed systems - the Edge Length and the Critical Length
- Eye diagram
- Short introduction to S Parameters
- Simulation examples

2. Fundamentals of Transmission Lines (TLs)

- Definition and fundamental structure
- Transmission Line Theory and the Telegraph Equations
- Types of Transmission Lines
- Transmission Line Model, Signal Current, Return Current (direction of voltage propagation, direction of signal current flow), Displacement Current
- Return Current distribution in the reference plane(s)
- Local impedance vs Characteristic Impedance and the impact of the Rise time
- Impedance mismatch: Reflection/Transmission Coefficients
- Multiple Reflections Analysis
- ISI due to reflections: reasons and practical design guidelines to reduce/eliminate
- Fundamentals of Microstrip and Stripline
- Simulation and measurement examples

3. Topologies

- Topology types: Point to Point, Daisy chain, Branched (T/Star)
- The influence of the topology on SI
- Practical guidelines to design branched topologies
- The Quarter Wave Stub Resonance
- Daisy Chain: short stubs widely Spaced and the package capacitance effect (time/frequency domain analysis)
- Short stubs Narrow Spacing and the effect on the characteristic impedance
- Simulation examples – DDR4

4. Terminations Techniques

- When is termination needed and effective? and when not?
- Considerations on how to choose the right termination
- Termination Types: End (parallel) Termination, Fly-by, R-C Termination, Thevenin (split) Termination, Vtt termination, Even and Odd mode Termination, Source Termination, Middle (junction) Termination
- Terminations for Multi Giga b/s data rates
- Simulation examples

5. Coupled Transmission Lines Theory (CrossTalk-XTALK)

- The Physical principles of the coupling mechanisms
- Inductance, Capacitance and Impedance Matrices of coupled TLs.
- XTALK in view of the return current and the influence of close planes
- NEXT and saturation length
- FEXT in Stripline and Microstrip
- BroadSide Coupling and practical ways to decrease it
- Differential crosstalk
- Multi Lane routing Considerations in Stripline and Microstrip
- ISI due to XTALK
- How much XTALK is too much?
- Common Techniques to Minimize XTALK
- Simulation and Measurement examples
- Summary and Design Guidelines.

6. Mode Conversion

- What is Mode Conversion and what are the causes for it?
- Mode Conversion: Why do we care?
- The Differential and the Common Signals
- Even and Odd modes in interconnects
- Effects of coupling on TL Properties in Even & Odd Modes - physical principles and analysis
- Velocity Variations due to Coupling and the effect on SI
- Termination of Odd/Even modes
- Tight vs Loose coupling differential pair design
- Serpentine design considerations
- ISI due to Mode Conversion
- Mode Conversion and Radiation
- How much Mode Conversion is too much?
- Simulation and Measurement examples
- Summary and Design Guidelines.

7. Vias & Connectors

Vias

- Inductance and Capacitance of a via - First Order Approximation
- Different Types of Vias in a Multi-layer Board
- Via design for Multi Giga b/s data rates
- Via's Impedance: elements affecting the via impedance, reflections from via and how to practically match the via?
- Tools to design the via impedance
- Via's Stub: physical principle and practical ways to reduce/eliminate the stub effect
- Via Time/frequency domain analysis
- Simulation examples
- Design Guidelines for via operating at Multi Giga b/s data rates

Connectors

- The pin Series and Mutual Inductance - First Order Approximation
- Effects of Inductive Coupling in the Connector
- Power Bounce in connectors
- Important connector properties at high speed and how to choose the right connector?
- How to check the connector's datasheet?
- Connector's Layout considerations at Multi Giga b/s data rates
- The connector's pad impedance mismatch and practical ways to match it
- Correct connector pin assignment at high speed
- Design and Layout Guidelines

8. Lossy Transmission Lines

- Path of least resistance vs path of least inductance
- Skin Effect: physical principle and effects. The Proximity Effect.
- AC resistance as function of frequency (the smooth conductor model)
- Reasons and models for Surface Roughness
- Signal Conductor and Reference Plane attenuation due to losses - 1st Order approximation
- The effect of Narrow Return Plane
- Dielectric losses: physical principles, model, material properties that affect dielectric losses, D_f (tangent delta) in different materials
- Attenuation due to dielectric loss - 1st order approximation
- The Total Attenuation
- ISI due to Losses – Rise time degradation
- The Characteristic Impedance in Lossy TLs.
- Advantages of losses
- Practical guidelines on how to design low attenuation channels operating at Multi Giga b/s rates.

9. Return Path (Ground) Bounce (RPB)

- Types of Return Path Discontinuities
- Non Continuous High Inductive Return Path Discontinuities:

(1) Signals Changing Reference Planes and the Return Path Bounce

- The impedance profile in the cavity (w/wo VRM)
- The cavity spreading inductance, self-resonance of the cavity, cavity modes
- The Impedance profile of the cavity: Why do we care?
- Periodic (sinusoidal) jitter
- Reducing the cavity impedance, controlled ESR caps
- Differential and common signals changing reference planes
- Reducing the cavity noise - design guidelines

(2) Signals Referenced to a Power or a Ground Plane and the Return Path Bounce

- Different reference planes for microstrip and stripline and the effects on the RPB
- The correct reference plane(s) in multi-voltage designs.
- Design guidelines to decrease RPB

(3) Signals (Single Ended, Differential and Common) Traversing a Finite Gap in the Reference Plane and the Return Path Bounce

- The physical principle, the gap inductance and the effects on SI.
- The inductive XTALK over the gap.
- Guidelines for reducing the gap effects on SI

(4) Analysis of Single-Ended and Differential Striplines Crossing Split Reference Planes in PCBs - Theory, Simulations, Measurements and Design Guidelines.

10. Jitter Analysis and Equalization

Jitter

- Overview
- The Time Interval Error (TIE)
- Jitter types, their sources and characteristics: Random jitter, Duty Cycle Distortion (DCD), ISI, Periodic (Sinusoidal) Jitter, Bounded Uncorrelated jitter, Total jitter
- Jitter Budget, Bathtub, BER, Eye Pattern, Statistical Contours and Receiver Eye Mask
- The dual Dirac model for deterministic jitter
- Jitter description in specifications
- Simulation and specification examples.

Equalizers

- Principles of operation
- Location options along the channel
- DLE: basic architecture, taps (delay and weight), the role of Pre-Cursor and Post-Cursor taps
- Tx Equalization: Feed Forward Equalizer (FFE) - De-emphasis and Pre-emphasis

- Rx Equalization: Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE)
- Integration of Re-drivers in lossy TLs.
- Examples from common specifications
- Simulation and measurement examples.

11. Power Integrity

- What is Power Integrity?
- Reasons for DC (IR) drop and practical ways to decrease it
- Power Delivery Problems: Rail Collapse, Simultaneous Switching Noise (SSN), Power Ground Bounce.
- Components of the Complete Power Delivery Network - PDN (from VRM to die)
- Target Impedance
- Capacitor modeling
- PDN time/frequency domain design and analysis
- Example of PDN design and simulation tools in Time and Frequency domains
- Peaks in the PDN's impedance profile: sources, impact and ways to reduce them
- Practical Design Guidelines to design robust PDN on the PCB
- Simulation examples.



www.interlligent.com