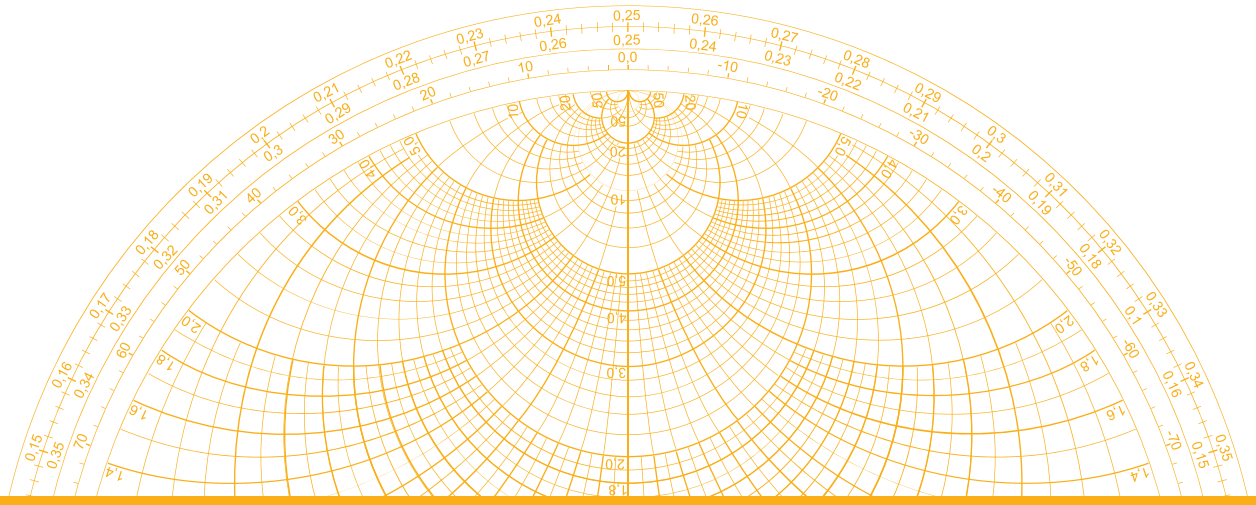
INTERLLIGENT
RF & Microwave Solutions

Signal and Power Integrity Course

4-day (36 study hours) course



RF Training

Test Equipment

Engineering Services

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RF is our Business... Signal us!

Signal and Power Integrity Course

Introduction

High speed digital signals are essentially broadband RF signals by nature, which need to propagate through a PCB or a system with a minimal distortion. The signal quality or Signal Integrity ("SI") can easily deteriorate due to multiple mechanisms, such as attenuation, crosstalk, mode conversion, poor impedance matching, jitter, dispersion and other causes. As a result, the overall Bit Error Rate (BER) is increased, while EMC test failures and product reliability problems emerge. These problems lead to extended development time, repetitive layouts, numerous reproductions and a waste of budget.
Moreover, Signal Integrity in high speed digital ICs is highly effected by the Power Supply's quality. This calls for strict Power Delivery Network (PDN) design and analysis from the die (silicon) to the Voltage Regulator Module on the PCB which is known as Power Integrity (PI).
This training course deals with Signal and Power integrity of high speed digital signals.

The topics include:

- Design and analysis of SI from PCB to system level and PI in the PCB level.
- Practical Design Guidelines for PCB design in multi restricted environment.
- Extensive SIPI theory and practice, demonstration of the studied material with the help of dozens of examples from simulations and measurements.
- Briefing on data sheets and common specifications
- Familiarizing with SIPI simulation and measurement tools.
- SI proof of design and failure investigations.
- Qualification in defining Layout instructions for proper SIPI.

Presenter

Dror Haviv received his Master of Science (M.Sc) degree in Electrical Engineering with honours from the Electromagnetic and Microwave programme at Ben-Gurion University (Beer-Sheva, Israel). He is one of Israel's leading Signal and Power Integrity (SI/PI) engineers and has years of design, analysis, measurement, and teaching experience in the Signal Integrity field behind him.

Today, Dror serves as a Technologist at the Signal and Power Integrity team at Western Digital ASIC platform engineering organisation. His job duties include flash controllers' Signal and Power Integrity design, silicon die and package co-design, modeling, system level Signal and Power Integrity simulations and correlation analysis of die/package SI/PI parameters between simulation and measurement results.

In the last decade, Dror served as the Signal Integrity Focal Point and Architect of the R&D division at Rafael. As a SI Architect, he designed, analysed, simulated, and measured dozens of systems and high-speed PCBs. As focal point, he has qualified, educated, trained, and supervised many engineers in the Signal Integrity field. Simultaneously, he served as a Senior Signal Integrity Cooperate Researcher and has conducted several research projects in the field. His research has been presented in conferences on Signal Integrity, both in Israel and abroad.

Target audience

All professional engineers that are involved in design, qualification and manufacturing of products that contain high speed digital signals, such as: board design, layout, SIPI, verification, system and process manufacturer engineers.

Course Duration

4 days (36 hours) from 8:30-17:30

Course Structure

The course includes extensive theoretical and practical background, examples from simulations and measurements, review of datasheets and specifications, open discussions etc.

Course Syllabus * Subject to changes *

1. Introduction

- Introduction to Signal Integrity
- The Band Width (BW) of deterministic digital signals, clocks, Knee Frequency, the fifth harmony
- The important harmonics in deterministic signals
- Power Spectral Density (PSD) of random digital data signals
- The Nyquist Frequency
- The BW of random digital signals (PRBS and Coded: 8b/10b, 64/66b)
- PAM4
- Properties of Electromagnetic TEM waves in PCBs
- Lumped vs Distributed systems - the Edge Length and the Critical Length
- Introduction to Eye diagram
- Short introduction to S Parameters
- Simulation examples

2. Transmission Lines (TLs) for High-Speed

- Definition and fundamental structure
- Transmission Line Theory
- Types of Transmission Lines
- Transmission Line Model, signal current, return current (direction of voltage propagation, direction of signal current flow), displacement current, inductance
- Return current distribution in the reference plane(s)
- Local impedance vs Characteristic impedance and the impact of the rise time
- Impedance mismatch: Reflection/Transmission coefficients
- Multiple reflections analysis
- Different methods for TDR, the influence of the rise time
- Introduction of Inter Symbol Interference (ISI)
- ISI due to reflections: reasons and practical design guidelines to reduce/eliminate
- How much Reflections is too much?
- Fundamentals of microstrip and stripline, the return current distribution
- Simulation and measurement examples

3. Terminations Techniques

- When is termination needed and effective? and when not?
- Considerations on how to choose the right termination: current consumption, SNR, power consumption, BOM, driver output impedance dependency, termination's location
- Termination types: End (parallel) Termination, Fly-by, R-C Termination, Thevenin (split) Termination, CTT termination, Source Termination for voltage and current drivers
- AC Coupling: DC block role, the role in Rx detection, principles and where to place?
- Terminations for multi Giga b/s data rates - ODT
- Simulation examples

4. Topologies

- Topology types: Point to Point, Daisy chain, Branched (T/Star)
- Symmetric vs asymmetric T topology
- The influence of the topology on signal integrity
- Practical guidelines to design branched topologies
- The Quarter Wave Stub Resonator: the resonance frequencies
- The stub length vs the data rate
- Simulation examples - DDR4: DBI, V_{REFDQ}

5. Coupled Transmission Lines Theory (Cross-Talk)

- The Physical principles of the coupling mechanisms and the electrical models
- Inductance, capacitance and impedance matrices of coupled TLs
- XTALK in view of the return current and the influence of the distance of the return planes
- NEXT in different transmission line lengths and the saturation length
- NEXT and FEXT in stripline and microstrip
- Broad-Side Coupling and practical ways to decrease it
- Differential crosstalk: loosely vs tightly coupled differential pairs
- Differential crosstalk: time domain analysis
- Multi lane routing XTALK considerations in stripline and microstrip NEXT and FEXT in lossy TLs
- How much XTALK is too much?
- Common techniques to minimize XTALK
- Simulation and measurement examples
- Summary and design guidelines

6. Mode Conversion

- The superposition of differential and common signals
- What is Mode Conversion and what are the causes for it?
- Dielectric constant skew – types of glass fabric
- The Differential and the Common Signals
- Even and Odd modes in interconnects
- Effects of coupling on TL properties in Even & Odd Modes - physical principles and analysis
- Even mode and Odd mode impedance, common and differential impedance
- Velocity and impedance variations due to coupling and the effect on signal integrity
- Termination of Odd/Even modes
- Tightly vs loosely coupling differential pair design
- Mode Conversion: 3 reasons why do we care: ISI, differential signal distortion, radiation
- How much intra-pair skew is too much?
- Serpentine design considerations
- ISI due to Mode Conversion
- Mode Conversion and radiation
- How much Mode Conversion is too much?
- FEXT in microstrip
- Simulation and measurement examples
- Summary and design guidelines

7. Vertical Interconnect Access (via) and Connectors

Vias

- Different types of vias in a multi-layer board, via manufacturing, via structure
- via length vs rise time
- via impedance and reflection ISI
- Inductance of a via: first order approximation, the effect on signal and power integrity
- via design for multi Giga b/s data rates: the transmission line model and the 3D model
- via's local impedance: elements affecting the via impedance, reflections from via and how to practically match the via?
- 2.5D and 3D methods to design the via impedance
- via's stub: physical principle, resonance frequencies and practical ways to reduce/eliminate the stub effect
- via time/frequency domain analysis
- Simulation examples
- Design guidelines for via operating at multi Giga b/s data rates

Connectors

- Important connector properties at high speed and how to choose the right connector?
- How to check the connector's datasheet?
- Connector's layout design at multi Giga b/s data rates
- The connector's pad impedance mismatch and practical ways to match it
- Correct connector pin assignment at high speed
- Design and layout guidelines

8. Losses in Transmission Lines

- Return path of least resistance vs return path of least inductance
- Skin effect: physical principle, skin depth. The Proximity effect
- The smooth conductor model for AC resistance and the frequency dependency
- AC resistance approximation in microstrip and stripline
- Surface roughness: reasons, models (Hammerstad, Hemispherical, Huray), measurement parameters, calculation in 3D tools
- Signal conductor and reference plane attenuation due to losses - 1st order approximation
- Dielectric losses: physical principles, model, material properties that affect dielectric losses, Df (tangent delta) in different materials
- Attenuation due to dielectric loss - 1st order approximation
- The total attenuation and the effect of the trace width
- Causality and dispersion
- ISI due to losses – rise time degradation, data dependent jitter (DDJ)
- How much attenuation is too much?
- The characteristic impedance in long lossy TL
- Practical guidelines on how to design low attenuation channels operating at multi Giga b/s rates

9. Jitter Analysis and Equalization

Jitter

- Overview
- The Time Interval Error (TIE), TIE histogram, eye pattern
- Jitter types, their sources and characteristics: Random jitter (RJ), Duty Cycle Distortion (DCD), ISI, Periodic (Sinusoidal-SJ) Jitter, Bounded Uncorrelated jitter (BUJ)
- Total jitter – convolution of the RJ and the deterministic jitter (DJ)
- Jitter Budget: RJ and DJ
- Error calculations: Bathtub, BER, eye pattern, statistical contours and receiver eye mask
- RJ calculation for different BER
- The dual Dirac model for deterministic jitter
- Jitter description in specifications
- Simulation and specification examples

Equalizers

- Principles of operation
- Active vs passive equalizers
- Equalizers location options along the channel
- DLE: basic architecture, taps (delay and weight), Pre-cursor and Post-cursor taps
- Tx Equalization: Feed Forward Equalizer (FFE) - De-emphasis, Pre-shoot and Pre-emphasis
- Rx Equalization: Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE)
- Integration of Re-drivers in lossy TLs, advantages and downsides
- Re-drivers vs Re-timers
- Examples from common specifications
- Simulation and measurement examples

10. Power Integrity

- What is Power Integrity?
- Reasons for DC (IR) drop and practical ways to decrease it
- Power supply filtering: Ferrite, EMI and Common Mode Choke – principles of operation and considerations on how to choose the right filter
- ntegrated Circuit (IC) Fabrication: Front and Back End of Line, wire-bonds vs flip-chip, packaging
- Power Delivery Problems: Rail Collapse, Simultaneous Switching Noise (SSN), Power Ground Bounce, jitter
- Components of the complete Power Delivery Network - PDN (from VRM to die)
- Target Impedance
- Practical capacitor modeling, the self-resonance, anti-resonance
- PDN frequency domain design and analysis
- The role of each capacitor in the PDN
- The impedance peaks potential problem in the PDN
- Example of PDN design and simulation tools in frequency domain
- Peaks in the PDN's impedance profile: sources, impact and ways to reduce them
- Practical design guidelines to design robust PDN on the PCB
- Simulation examples in pre-layout and in post-layout stages

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